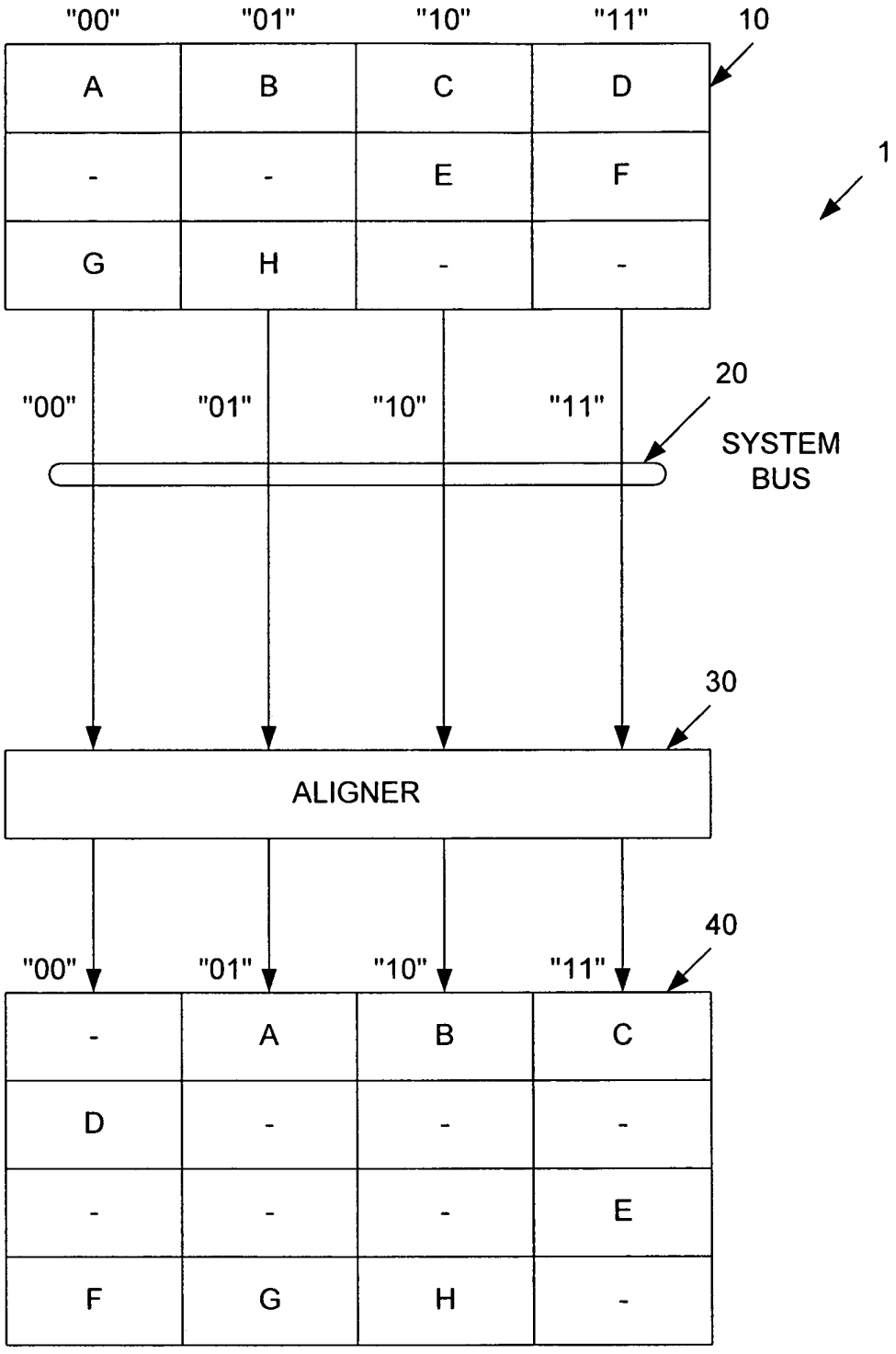


FIG. 1
(PRIOR ART)

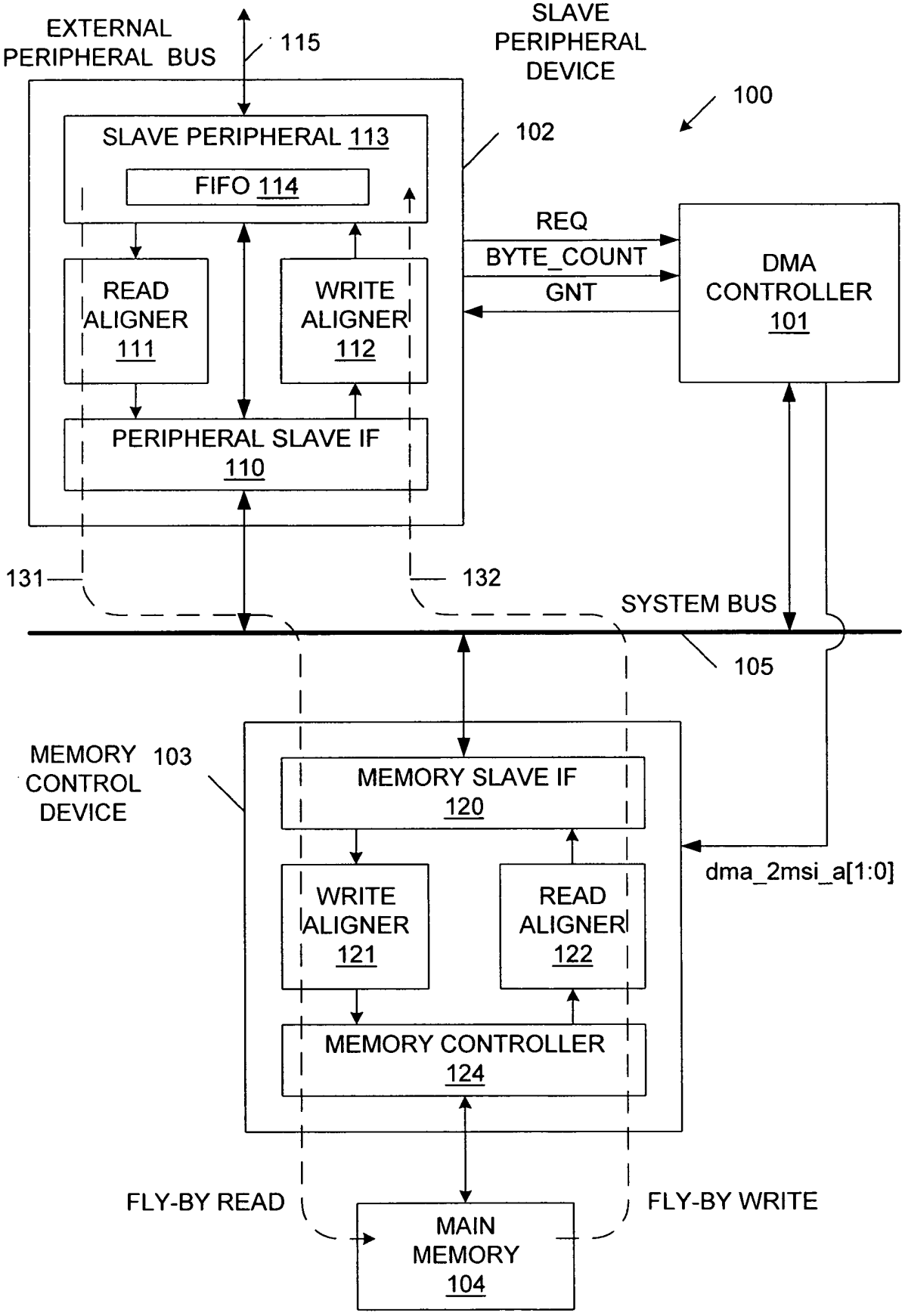

EXTERNAL PERIPHERAL BUS
115
SLAVE PERIPHERAL DEVICE
100
102
SLAVE PERIPHERAL 113
FIFO 114
READ ALIGNER 111
WRITE ALIGNER 112
PERIPHERAL SLAVE IF 110
REQ
BYTE_COUNT
GNT
DMA CONTROLLER 101
131
132
SYSTEM BUS
105
MEMORY CONTROL DEVICE
103
MEMORY SLAVE IF 120
WRITE ALIGNER 121
READ ALIGNER 122
MEMORY CONTROLLER 124
dma_2msi_a[1:0]
FLY-BY READ
FLY-BY WRITE
MAIN MEMORY 104

FIG. 2

DATA IN FIFO 114

	00	01	10	11
201	x	x	A	B
202	C	D	E	F
203	G	H	I	J
204	K	L	M	N
205	O	P	Q	R
206	S	T	U	V
207	W	X	Y	Z

114

FIG. 3

DATA ON SYSTEM BUS 105

	00	01	10	11
301	A	B	C	D
302	E	F	G	H
303	I	J	K	L
304	M	N	O	P
305	Q	R	S	T
306	U	V	W	X
307	Y	Z	x	x

105

FIG. 4

DATA TO MEMORY 104

	00	01	10	11
401	x	x	x	A
402	B	C	D	E
403	F	G	H	I
404	J	K	L	M
405	N	O	P	Q
406	R	S	T	U
407	V	W	X	Y
408	Z	x	x	x

104

FIG. 5

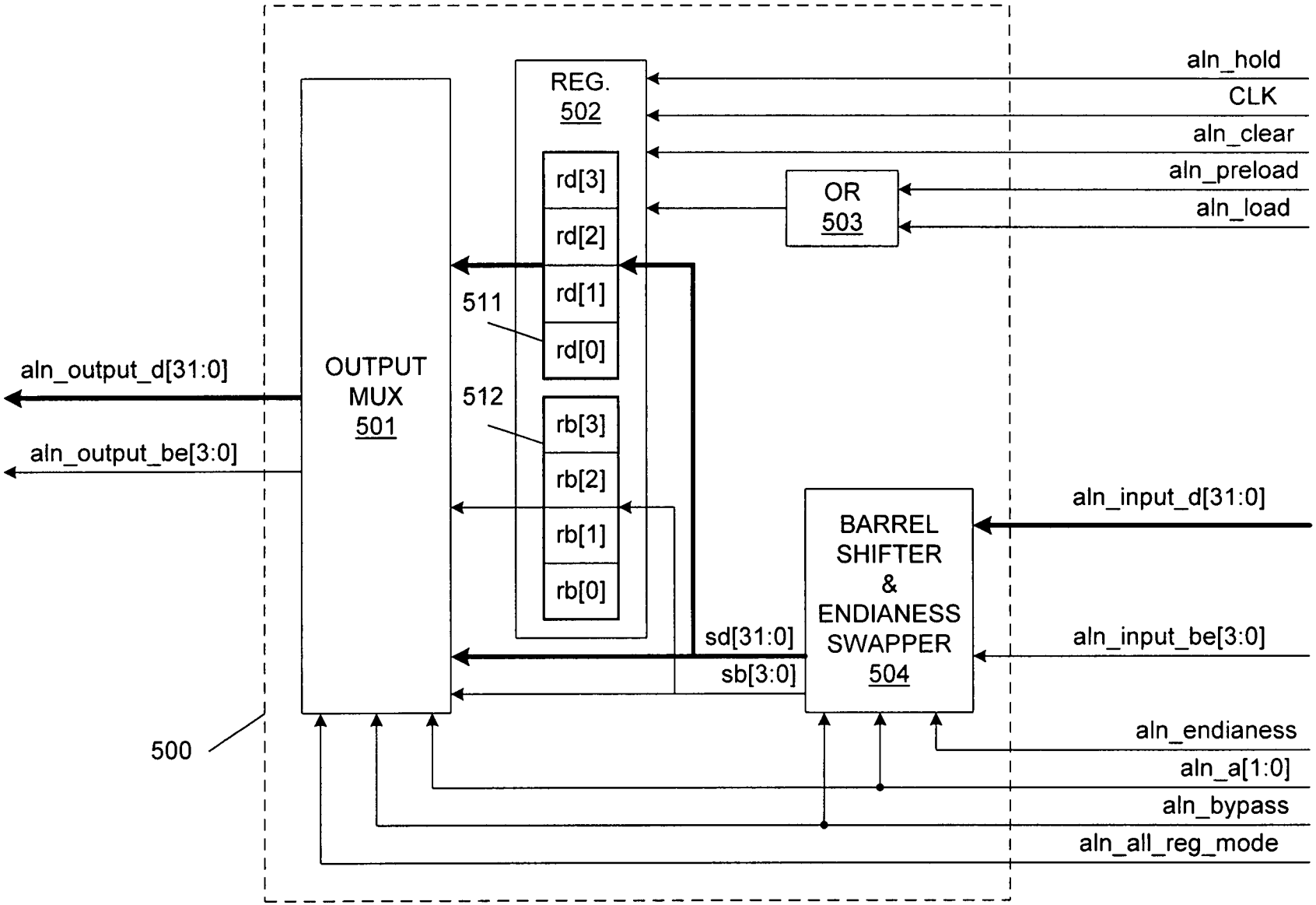

aln_hold
CLK
aln_clear
aln_preload
aln_load
REG.
502
OR
503
rd[3]
rd[2]
rd[1]
rd[0]
511
512
rb[3]
rb[2]
rb[1]
rb[0]
aln_output_d[31:0]
aln_output_be[3:0]
OUTPUT
MUX
501
sd[31:0]
sb[3:0]
BARREL
SHIFTER
&
ENDIANESS
SWAPPER
504
aln_input_d[31:0]
aln_input_be[3:0]
aln_endianess
aln_a[1:0]
aln_bypass
aln_all_reg_mode
500

FIG. 6

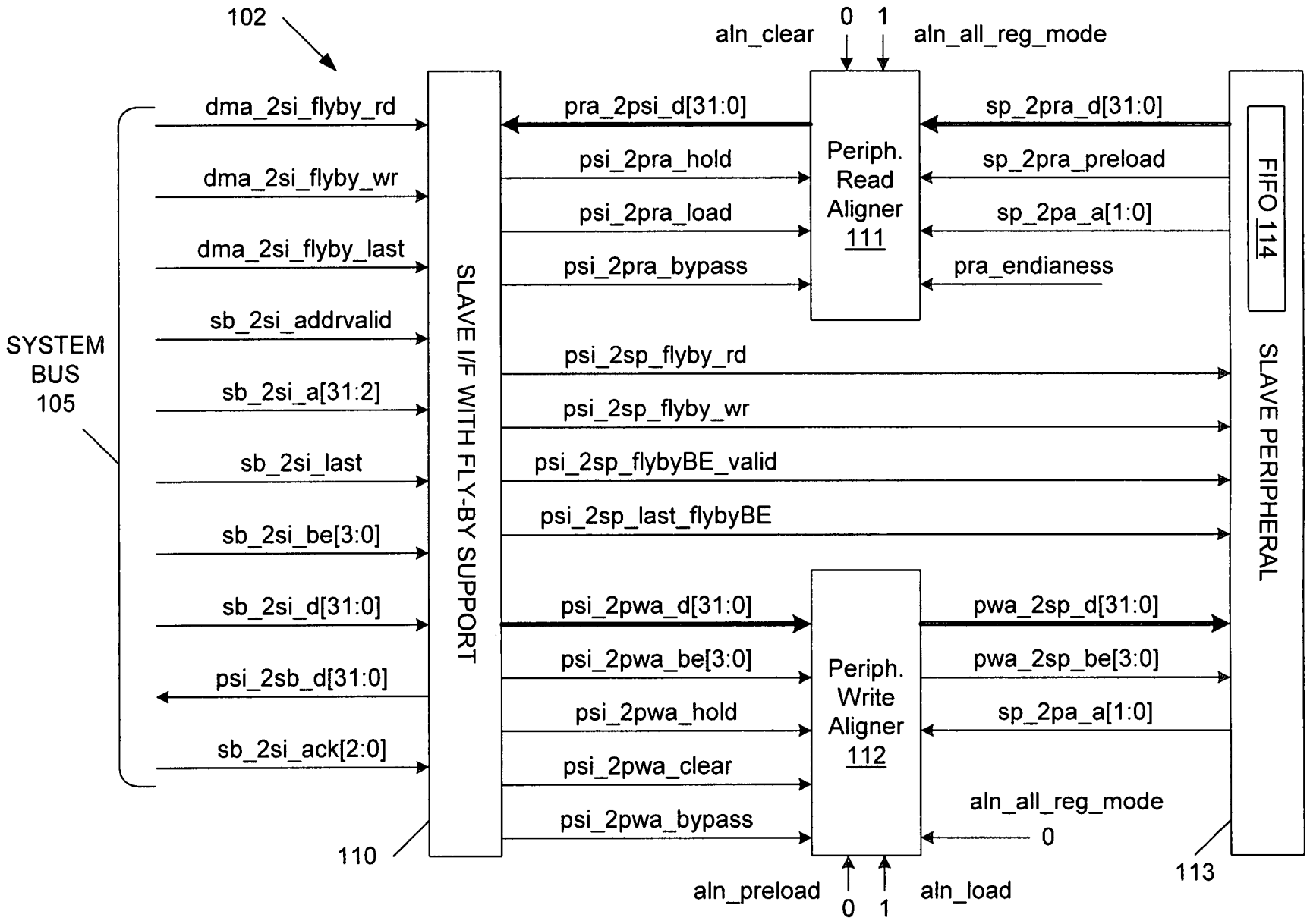
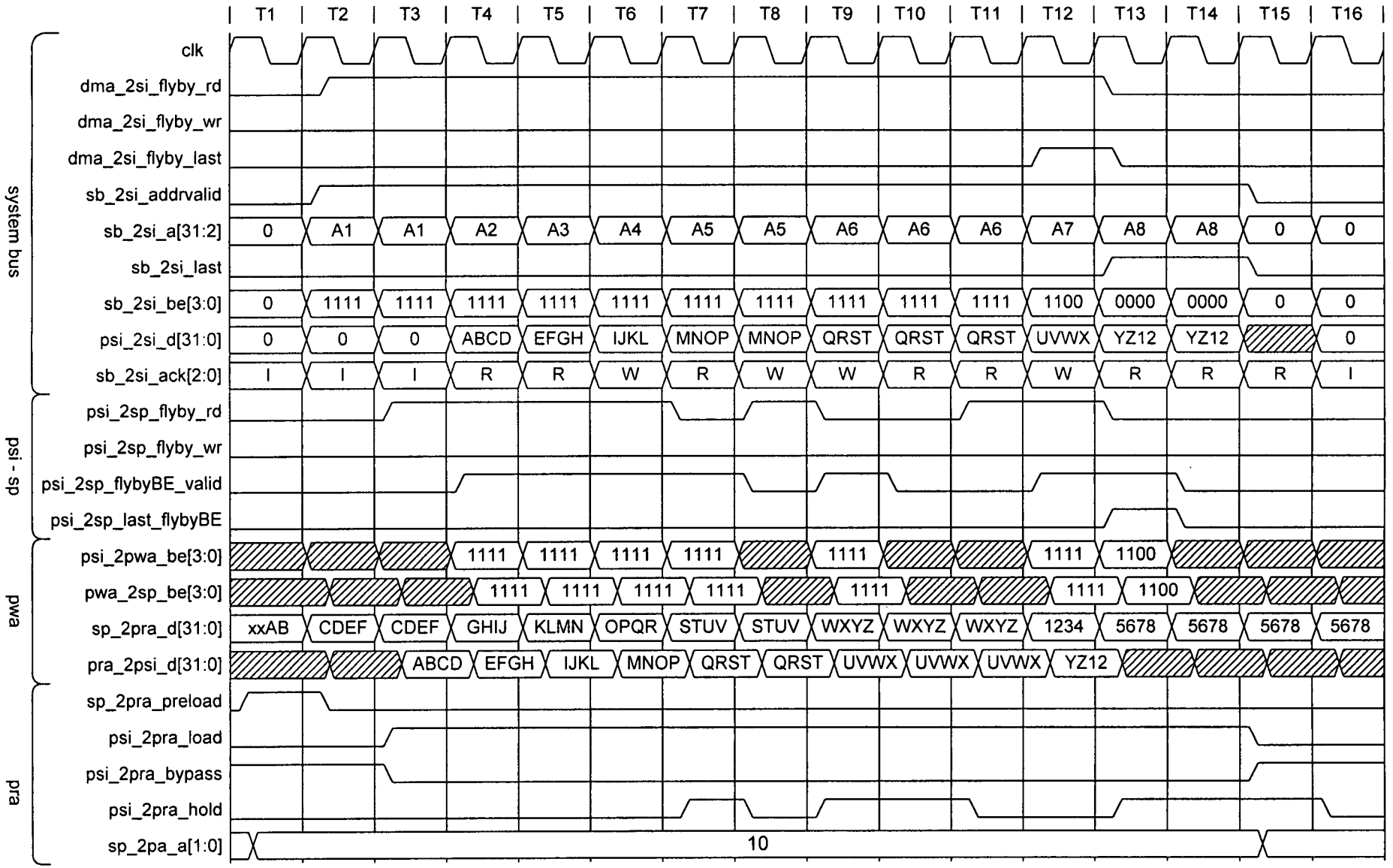

102
aln_clear
0
1
aln_all_reg_mode
dma_2si_flyby_rd
dma_2si_flyby_wr
dma_2si_flyby_last
sb_2si_addrvalid
sb_2si_a[31:2]
sb_2si_last
sb_2si_be[3:0]
sb_2si_d[31:0]
psi_2sb_d[31:0]
sb_2si_ack[2:0]
SYSTEM BUS 105
SLAVE I/F WITH FLY-BY SUPPORT
110
pra_2psi_d[31:0]
psi_2pra_hold
psi_2pra_load
psi_2pra_bypass
Periph. Read Aligner 111
sp_2pra_d[31:0]
sp_2pra_preload
sp_2pa_a[1:0]
pra_endianess
FIFO 114
SLAVE PERIPHERAL
113
psi_2sp_flyby_rd
psi_2sp_flyby_wr
psi_2sp_flybyBE_valid
psi_2sp_last_flybyBE
psi_2pwa_d[31:0]
psi_2pwa_be[3:0]
psi_2pwa_hold
psi_2pwa_clear
psi_2pwa_bypass
Periph. Write Aligner 112
pwa_2sp_d[31:0]
pwa_2sp_be[3:0]
sp_2pa_a[1:0]
aln_all_reg_mode
0
aln_preload
0
1
aln_load

FIG. 7



psi_2pwa_hold = 0

psi_2pwa_clear = 1

psi_2pwa_bypass =1

FLY-BY READ (SLAVE PERIPHERAL DEVICE 102)

FIG. 8

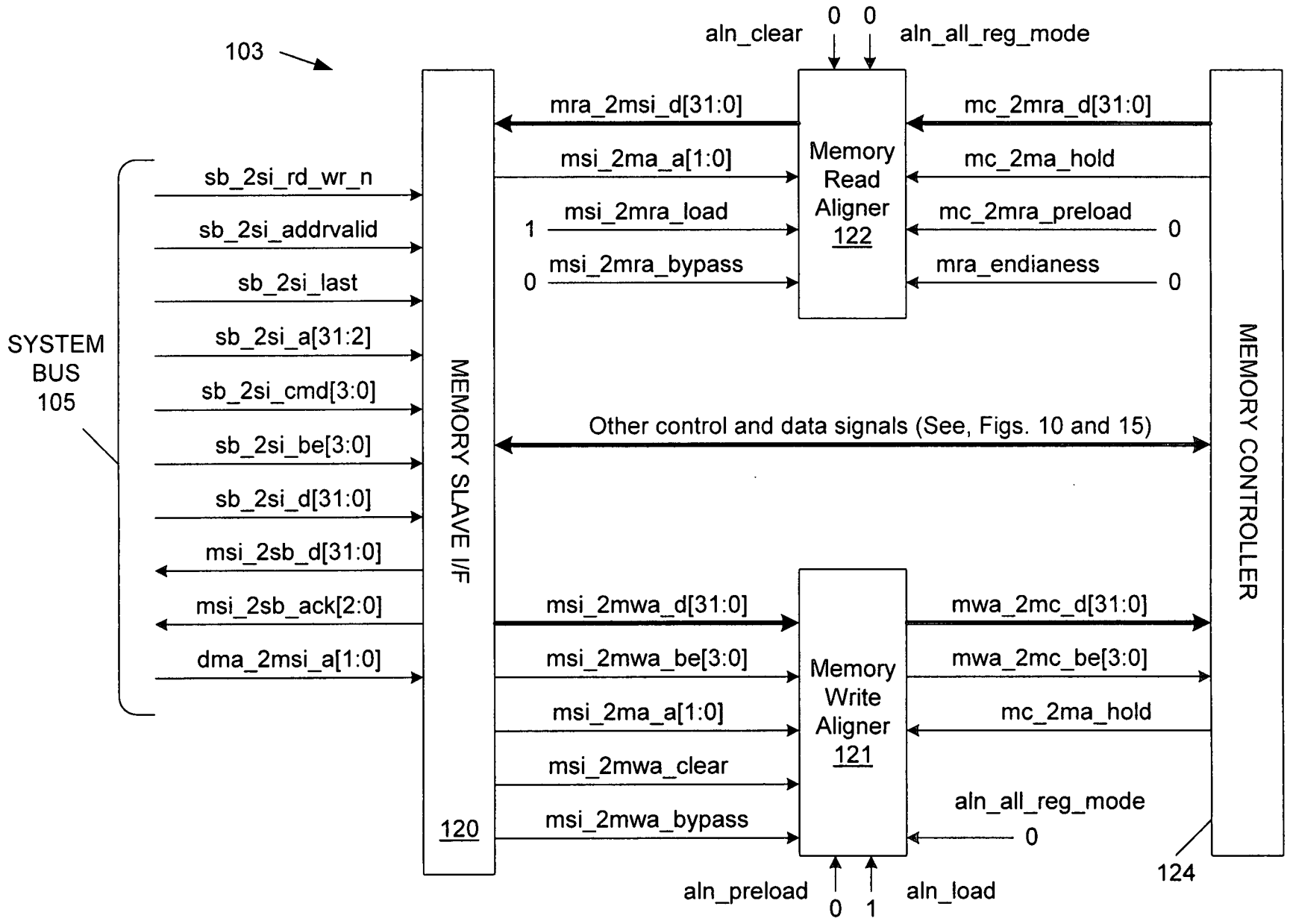
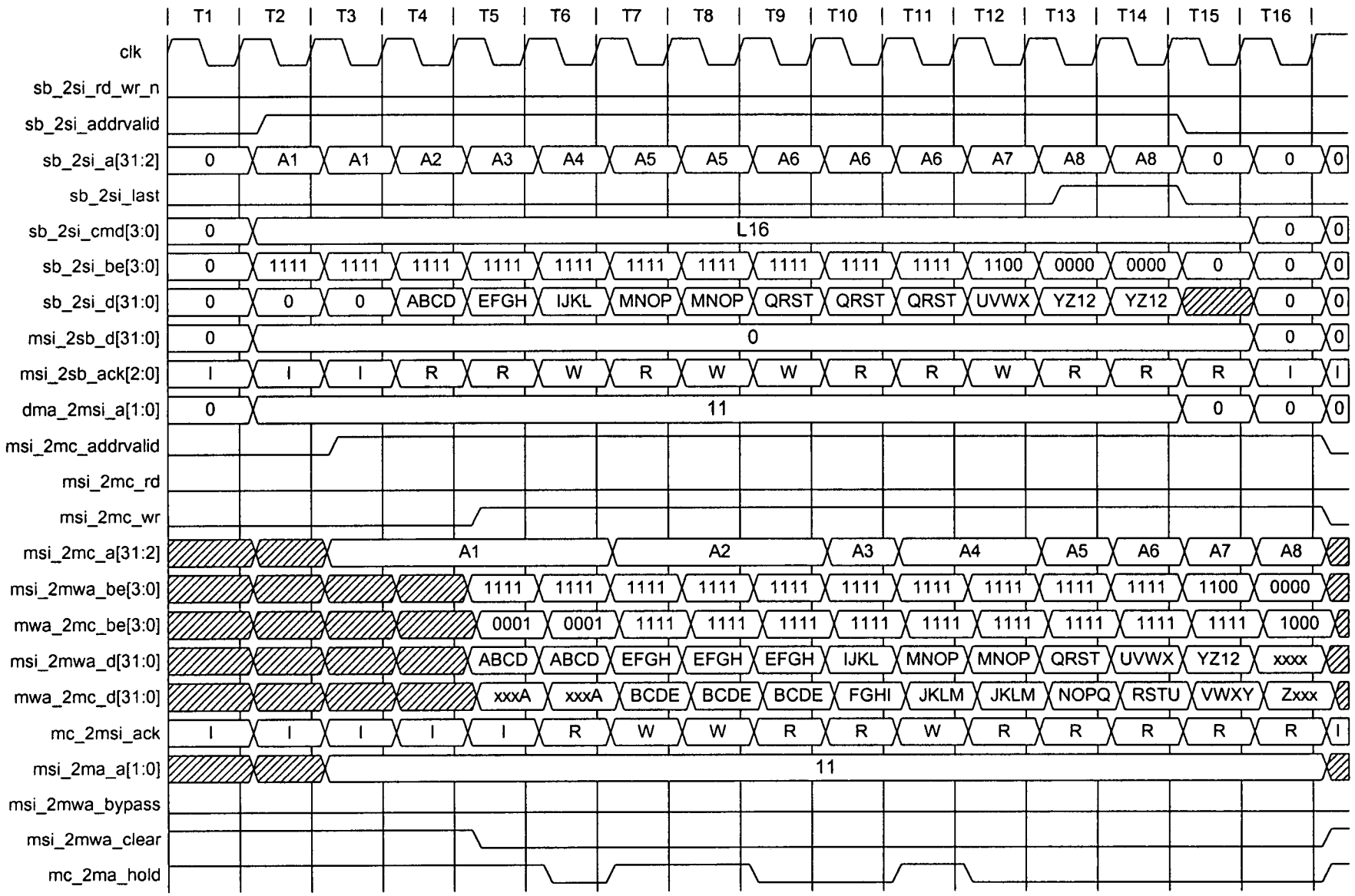
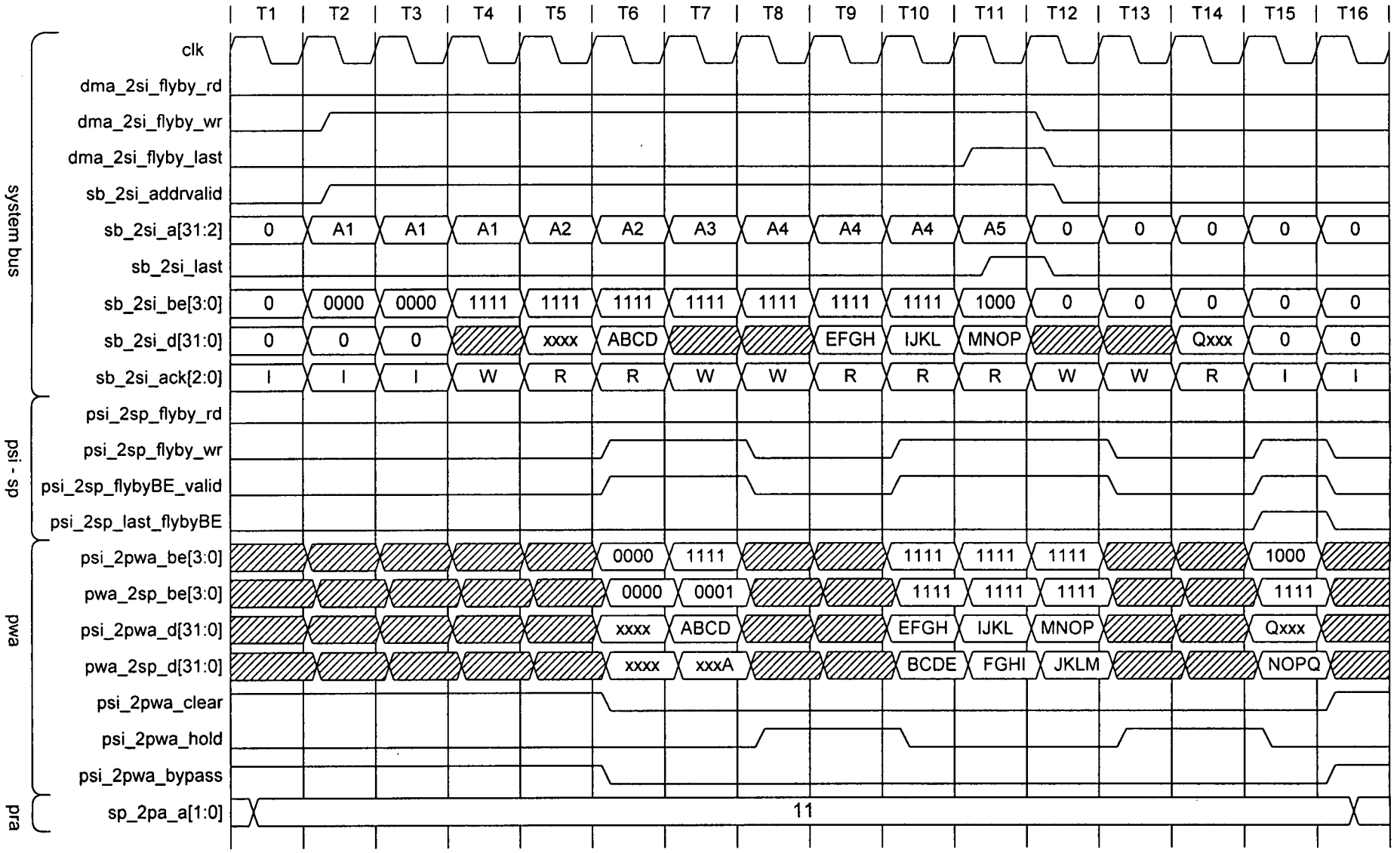

103
aln_clear
0
0
aln_all_reg_mode
mra_2msi_d[31:0]
mc_2mra_d[31:0]
msi_2ma_a[1:0]
mc_2ma_hold
Memory Read Aligner 122
msi_2mra_load
1
mc_2mra_preload
0
msi_2mra_bypass
0
mra_endianess
0
SYSTEM BUS 105
sb_2si_rd_wr_n
sb_2si_addrvalid
sb_2si_last
sb_2si_a[31:2]
sb_2si_cmd[3:0]
sb_2si_be[3:0]
sb_2si_d[31:0]
msi_2sb_d[31:0]
msi_2sb_ack[2:0]
dma_2msi_a[1:0]
MEMORY SLAVE I/F
120
Other control and data signals (See, Figs. 10 and 15)
MEMORY CONTROLLER
msi_2mwa_d[31:0]
mwa_2mc_d[31:0]
msi_2mwa_be[3:0]
mwa_2mc_be[3:0]
msi_2ma_a[1:0]
mc_2ma_hold
Memory Write Aligner 121
msi_2mwa_clear
aln_all_reg_mode
msi_2mwa_bypass
0
124
aln_preload
0
1
aln_load

FIG. 9



FLY-BY READ (MEMORY CONTROL DEVICE 103)

FIG. 10



psi_2pra_hold = 0
psi_2pra_load = 0
psi_2pra_preload = 0
psi_2pra_bypass =1
psi_2sb_d[31:0] = 0

FLY-BY WRITE (SLAVE PERIPHERAL DEVICE 102)

FIG. 11

DATA IN MAIN MEMORY 104

ADDR	00	01	10	11
A1	x	A	B	C
A2	D	E	F	G
A3	H	I	J	K
A4	L	M	N	O
A5	P	Q	x	x
A6	x	x	x	x

104

FIG. 12

DATA, ADDRESS AND BYTE-ENABLES ON SYSTEM BUS 105

ADDR	00	01	10	11	BE
A1	x	x	x	x	0000
A1	A	B	C	D	1111
A2	E	F	G	H	1111
A3	I	J	K	L	1111
A4	M	N	O	P	1111
A5	Q	x	x	x	1000

105

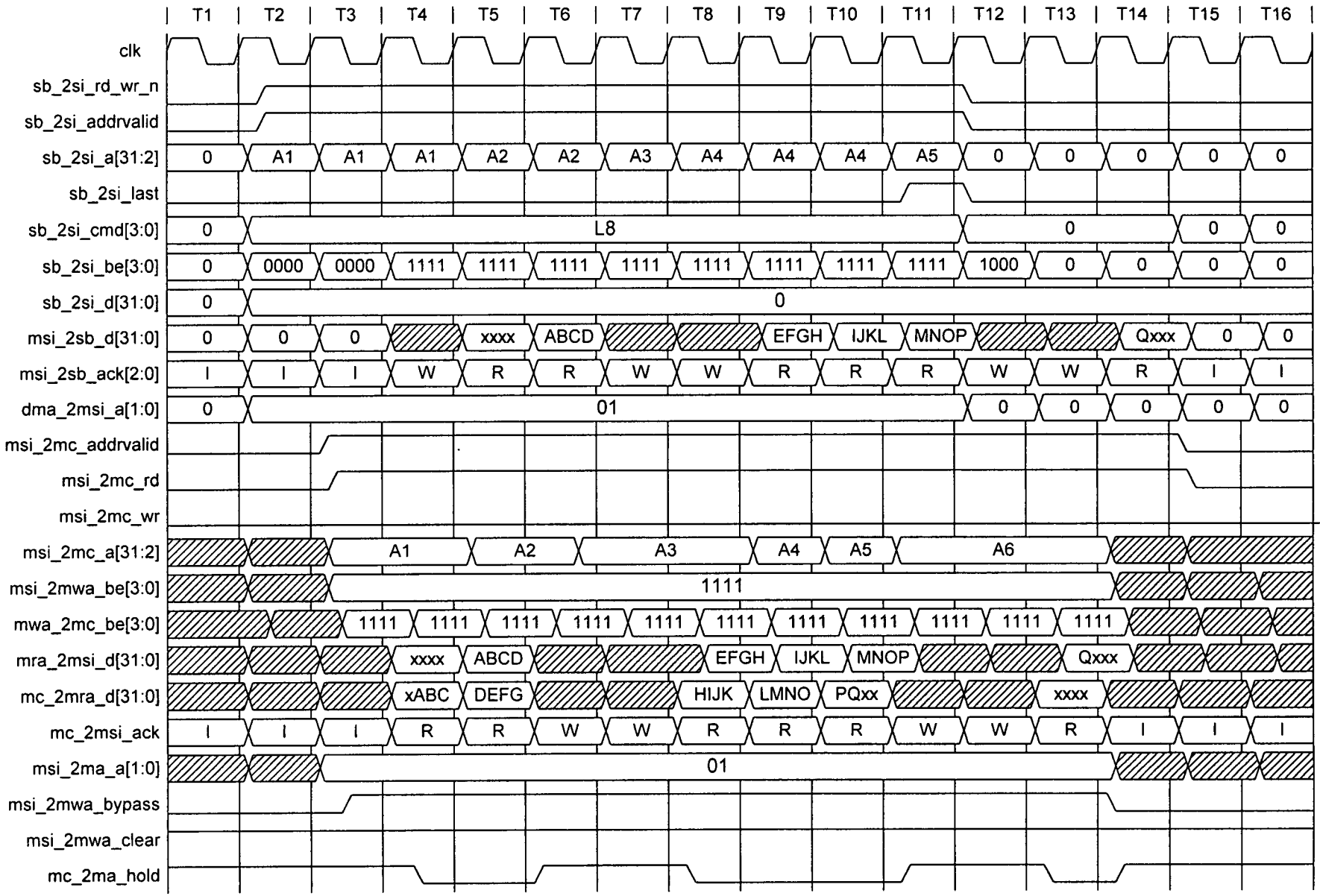
FIG. 13

DATA AND BYTE ENABLES RECEIVED BY SLAVE PERIPHERAL 113

00	01	10	11	BE
x	x	x	x	0000
x	x	x	A	0001
B	C	D	E	1111
F	G	H	I	1111
J	K	L	M	1111
N	O	P	Q	1111

113

FIG. 14



FLY-BY WRITE (MEMORY CONTROL DEVICE 103)

FIG. 15